AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of fabricating an integrated circuit comprising:

forming a diffusion barrier layer pattern on a semiconductor substrate;

forming a SOG layer containing impurities, including either one of a p-type impurity and an n-type impurity on the entire surface of the semiconductor substrate;

additionally implanting impurity ions into portions of the SOG layer formed on the diffusion barrier layer and the semiconductor substrate by a plasma ion implantation method to increase the concentration of impurities in the SOG layer; and

diffusing the impurity ions contained in the SOG layer having the increased concentration of impurities into the semiconductor substrate by a solid phase diffusion method to form shallow junctions.

2. (Original) The method of claim 1, wherein the SOG layer is formed by spin-coating and densifying a liquid silicate glass including one of P, B, In, As, and Sb doping elements.

3. (Original) The method of claim 1, wherein the SOG layer is formed by chemical vapor deposition (CVD) using a compound gas including SiH_4, O_2, and one of P, B, In, As, and Sb doping elements.

4. (Original) The method of claim 1, wherein the concentration of impurities of the SOG layer is increased using a plasma ion implanter including a Plasma Immersion Ion Implanter (PIII) and an Ion Shower Implanter (ISI).

5. (Original) The method of claim 1, wherein the maximum impurity implantation concentration of the SOG layer additionally implanted with the impurity ions is adjusted to 10^{19} – $10^{23}cm^{-3}$.

6. (Canceled).

7. (Original) The method of claim 1, wherein the shallow junctions are formed by the solid phase diffusion method using one of rapid thermal annealing (RTA), spike annealing, and laser annealing.

8. (Original) The method of claim 7, wherein in the RTA, the semiconductor substrate on which the SOG layer having the increased concentration of impurities is formed is rapidly thermally annealed at a temperature of 950 – 1150 °C for 1 – 1000 seconds in an inert gas atmosphere.

9. (Original) The method of claim 7, wherein in the spike annealing, the semiconductor substrate on which the SOG layer having the increased concentration of impurities is formed is rapidly thermally annealed at a temperature of 950 – 1200 °C in an inert gas atmosphere.

10. (Original) The method of claim 1, wherein the shallow junctions have a doping depth of 50nm or less on the semiconductor substrate and a doping concentration of $10^{18} - 10^{22}cm^{-3}$.

11. (Currently Amended) A method of fabricating an integrated circuit comprising:

forming a gate pattern on a semiconductor substrate;

forming a SOG layer containing impurities, including either one of a p-type impurity and an n-type impurity on the entire surface of the semiconductor substrate;

additionally implanting impurity ions into portions of the SOG layer formed on the gate pattern and the semiconductor substrate by a plasma ion implantation method to selectively increase the concentration of impurities of the SOG layer; and

diffusing the impurity ions contained in the SOG layer into the semiconductor substrate by a solid phase diffusion method to form shallow junctions having a LDD region self-aligned underneath both sidewalls of the gate pattern and a highly doped source/drain region adjacent to the LDD region.

12. (Original) The method of claim 11, wherein the ratio of the thickness of the SOG layer to the height of a gate electrode constituting the gate pattern is between 1:1.5 and 1:10.

13. (Original) The method of claim 11, wherein the SOG layer is formed by spin-coating and densifying a liquid silicate glass including one of P, B, In, As, and Sb doping elements.

14. (Original) The method of claim 11, wherein the SOG layer is formed by CVD using a compound gas including SiH_4, O_2, and one of P, B, In, As, and Sb doping elements.

15. (Original) The method of claim 11, wherein the concentration of impurities of the SOG layer is selectively increased using a plasma ion implanter including a PIII or an ISI.

16. (Original) The method of claim 11, wherein the maximum impurity implantation concentration of the SOG layer additionally implanted with the impurity ions is adjusted to $10^{19} - 10^{23}cm^{-3}$.

17. (Original) The method of claim 11, wherein the shallow junctions are formed by the solid phase diffusion method using one of rapid thermal annealing (RTA), spike annealing, and laser annealing.

18. (Original) The method of claim 17, wherein in the RTA, the semiconductor substrate on which the SOG layer having the increased concentration of impurities is formed is rapidly thermally annealed at a temperature of 950 – 1150 °C for 1 – 1000 seconds in an inert gas atmosphere.

19. (Original) The method of claim 17, wherein in the spike annealing, the semiconductor substrate on which the SOG layer having the increased concentration of impurities is formed is rapidly thermally annealed at a temperature of 950 – 1200 °C in an inert gas atmosphere.

20. (Original) The method of claim 11, wherein the shallow junctions have a doping depth of 50nm or less on the semiconductor substrate and a doping concentration of $10^{18} - 10^{22} cm^{-3}$.